IN THE TITLE

Please replace the title with the following:

--SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY HANDLER--.

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning on page 4, line 20 is amended as follows:

The processor 104 can be any type of processor. The processor [404] 104 may be compatible with, but is not limited to, processors such as an Intel® architecture processor, manufactured by Intel Corporation of Santa Clara, California, the assignee of the present invention. The processor 104 can use 32 bit instructions or 64 bit instructions. The processor 104 may be pipelined. The processor 104 executes code from the memory hierarchy 102. The processor 104 may be one of a number of processors in a computer system.

The paragraph beginning on page 8, line 3 is amended as follows:

Figure 2 discloses a system 200 for reproducing executions according to one embodiment of the invention. The system includes a storage element 201, a memory hierarchy 202, a system bus 203, a processor 204, a port 205, trace hardware 206 and a host system 207. The storage element 201 can be any device capable of storing data. For example, the storage element can be dynamic memory or a hard drive. The storage element 201 can be physically located away from the other elements of the system.

The paragraph beginning on page 15, line 3 is amended as follows:

Figure 4 is a block diagram of one embodiment of a computer system 400 that is suitable for implementing the present invention. The disclosed embodiment of computer system 400

includes a plurality of processors [410] 410(1)-410(n) that are coupled to system logic 430 through a processor bus 420. A system memory 440 is coupled to system logic [120] 430 through bus 450. A non-volatile memory 470 and one or more peripheral devices 480(1)-480(j) (collectively, devices 480) are coupled to system logic 430 through peripheral bus 460. Peripheral bus 460 represents, for example, one or more peripheral component interconnect (PCI) buses, industry standard architecture (ISA) buses, extended ISA (EISA) buses, and comparable peripheral buses. Non-volatile memory 470 may be a static memory device such as a read only memory (ROM) or flash memory. Peripheral devices 480 include, for example, a keyboard, mouse or other pointing devices, mass storage devices such as hard drives and digital video discs (DVD), a display, and the like. These devices, together with system logic 430 define the computing platform for system 400.

The paragraph beginning on page 15, line 17 is amended as follows:

For the disclosed embodiment of system 400, processors [410] 410(1)-410(n) may execute code or routines stored in system memory 440. The processor also executes code from the non-volatile memory 470. Additionally, the processor may execute code from an instruction cache.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 3, 4-6, 7, 10, 17, 20, and 23. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A system comprising:

a storage element;

a memory hierarchy coupled to the storage element;

a processor coupled to the memory hierarchy, wherein the processor is configured to test itself by repeatedly executing a plurality of instructions using a replay handler loaded into the